WHAT IS CLAIMED IS:

1. A non-volatile SONOS memory device comprising:

a semiconductor substrate including a source region and a drain region;

a channel formed in the semiconductor substrate between the source region and the drain region, the channel being a stepped channel comprising at least a top part, an inclined part and a bottom part, the top part being adjacent to the source region and the bottom part being adjacent to the drain region;

a gate insulation layer including a nitride layer formed over the channel, the nitride layer being formed over both the inclined part and the bottom part; and

a gate electrode formed over the gate insulation layer,

electrons being injected into the nitride layer through the inclined part of the channel.

2. The non-volatile SONOS memory device of claim 1, wherein the nitride layer is inserted in an oxide layer.

3. The non-volatile SONOS memory device as defined by claim 2, wherein the oxide layer comprises at least a first oxide layer and second oxide layer, and the nitride layer is disposed between the first oxide layer and the second oxide layer.

4. The non-volatile SONOS memory device as defined by claim 3, wherein the first oxide layer and the nitride layer are formed only over the bottom part and the inclined part of the channel.

5. The non-volatile SONOS memory device as defined by claim 1, wherein the inclined part of the channel is inclined by at least an angle of 30 degrees.

6. A method of fabricating a non-volatile SONOS memory device comprising the steps of:

forming a stepped pattern in a semiconductor substrate , the stepped pattern comprising a top part, an inclined part, and a bottom part;

forming an ONO insulation layer over the stepped pattern on the semiconductor substrate;

forming a conductive layer over the ONO insulation layer;

patterning the ONO insulation layer and the conductive layer to form a gate insulation layer and a gate electrode; and

forming a source region in the substrate at one side of the gate electrode and a drain region in the substrate at another side of the gate electrode.

7. The method of claim 6, wherein the gate insulation layer comprises a nitride layer, and the nitride layer is inserted in an oxide layer.

8. The method of claim 7, wherein the nitride layer is disposed over only the inclined and bottom parts of the channel.

9. The method of claim 6, wherein a step of forming the ONO insulation layer comprises the steps of:

forming a first oxide layer, a nitride layer and a second oxide layer sequentially on the semiconductor substrate;

removing the second oxide layer and the nitride layer formed on the top part;

removing the first oxide layer remaining on the top part and the second oxide layer remaining on the inclined part and the bottom part;

forming a third oxide layer over the semiconductor substrate, thereby covering the nitride layer and the first oxide layer remaining on the inclined part and the bottom part; and

annealing the semiconductor substrate.

10. The method of claim 9, wherein a step of removing the nitride layer and the second oxide layer formed on the top part comprises the steps of:

forming a photoresist pattern on the second oxide layer to cover only the inclined and bottom parts;

etching the nitride layer and the second oxide layer formed on the top part using the photoresist pattern as a mask; and

removing the photoresist pattern.

11. The method of claim 9, wherein the step of removing the first and second oxide layer layers comprises a wet etching process.

12. The method of claim 9, wherein the third oxide layer is a CVD oxide layer.

13. The method of claim 6, wherein the source region is adjacent to the top part and the drain region is adjacent to the bottom part.

14. A method of fabricating a non-volatile SONOS memory device comprising the steps of:

forming a stepped pattern in a semiconductor substrate, the stepped pattern comprising a top part, an inclined part, and a bottom part;

forming a first oxide layer layer, a nitride layer and a second oxide layer sequentially over the stepped pattern of the semiconductor substrate;

removing the nitride layer and the second oxide layer formed over the top part;

removing the first oxide layer remaining on the top part and the second oxide layer remaining on the inclined and bottom parts;

forming a third oxide layer over the semiconductor substrate, thereby covering the first oxide layer and the nitride layer remaining on the inclined and bottom parts;

annealing the semiconductor substrate;

forming a conductive layer on the third oxide layer;

patterning the conductive layer, the third oxide layer, the nitride layer, and the first oxide layer to form a gate insulation layer and a gate electrode; and

forming a source region in the substrate at one side of the gate electrode and a drain region in the substrate at another side of the gate electrode.

15. The method of claim 14, wherein a step of removing the nitride layer and the second oxide layer formed on the top part comprises the steps of:

forming a photoresist pattern over the second oxide layer to cover only the inclined and bottom parts;

etching the nitride layer and the second oxide layer formed over the top part using the photoresist pattern as a mask; and

removing the photoresist pattern.

16. The method of claim 14, wherein the step of removing the first oxide layer and the second oxide layer comprises a wet etching process.

17. The method of claim 14, wherein the third oxide layer is a CVD oxide layer.

18. The method of claim 14, wherein the source region is adjacent to the top part and the drain region is adjacent to the bottom part.